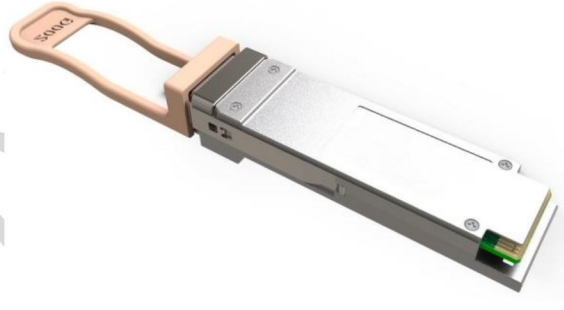
200G QSFP56 SR4 Optical Transceiver

C200Q00100SR402A

Product Specification

200G QSFP56 SR4 is a 4×50Gbps multi mode fiber, hot pluggable optical transceiver. The module integrates four parallel lanes with baud rate at 26.5625GBd each lane. It can transmit up to 70 m on fiber OM3 fiber or 100 m on OM4 fiber with FEC.



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Applications

- 200GBASE-SR4 Ethernet links
- Data centers

Features

- Compliant with IEEE Std 802.3bs, IEEE Std 802.3cm
- Compliant with 200G-SR4 optical specifications
- Compliant with SFF-8679
- Compliant with CMIS4.0 Management interface specifications
- 4x53.125Gb/s electrical interface (200GAUI-4)
- Reach up to 70m on MMF(OM3)
- Reach up to 100m on MMF(OM4)
- Single +3.3V power supply
- Case temperature range: 0 ~ +70℃
- Maximum power consumption 5W
- Single MPO12 connector
- RoHS complaint

Rev	Date	Modified by	Description
A	Jan 20,2020	Fay Tu	Initial Release

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Table1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	T_{STG}	-40	+85	°C
Supply Voltage	V_{CC}	0	4	V
Relative Humidity	RH	5% to 85% non-condensing		

Table2. Operating Conditions

Parameter	Symbol	Min	Max	Units
Case Temperature- Operating	T_{CASE}	0	70	°C
Supply Voltage	Vcc	3.14	3.46	V
Power Consumption	P_{DISS}		5	W
Pre-FEC Bit Error Ratio			$2.4x10^{-4}$	
Link Distance over OM4 Fiber			100	M
Link Distance over OM3 Fiber			70	M

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Table3. Transmitter Optical Specifications

Transmitter Parameter	Min	Typical	Max	Units
Signaling Rate, each lane		26.5625 ± 100 ppm		GBd
Center Wavelength Range	840	850	860	nm
Modulation Format		PAM4		
Average launch Power per lane	-6.5		4	dBm
RMS spectral width			0.6	nm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	-4.5		3	dBm
Average Launch Power per Lane @ TX Off State			-30	dBm
Launch Power in OMAouter minus TDECQ, each Lane	-5.9			dBm
Transmitter and Dispersion Eye Closure for PAM4, each Lane			4.5	dB
Extinction Ratio	3			dB
Optical Return Loss Tolerance			12	dB
Encircled flux at 4.5um			30	%
Encircled flux at 19um	86			%

Table4. Receiver Optical Specifications

Receiver Parameter	Min	Typical	Max	Units
Signaling Rate, each lane		26.5625 ± 100 ppm		
Lane Wavelength Range	840	850	860	nm
Modulation Format				
Damage Threshold	5			dBm
Average Receive Power, each lane	-8.4		4	dBm
Receiver Power, each lane (OMA)			3	dBm
Receiver Reflectance			-12	dB
Receiver sensitivity(OMA_{outer})each lane(SECQ=1.4dB)			-6.5	dBm
Stressed Receiver Sensitivity (OMA_{outer}), each lane			-3.4	dBm
Stressed Conditions for Stress Receiver Sensitivity				
Stressed Eye Closure for PAM4 (SECQ),Lane under Test		4.5		dB
SECQ-10log10(Ceq),each lane			4.5	
OMA_{outer} of each Aggressor Lane		3.0		dBm

Table5. Ordering Information

Product Description	Part Number
200G QSFP56 SR4 Module	C200Q00100SR402A

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QSFP56 Connector and Pinout Description

The electrical interface to the transceiver is a 38 pins edge connector. The 38 pins provide high speed data, low speed monitoring and control signals, I2C communication, power and ground connectivity. The top and bottom views of the connector are provided below, as well as a table outlining the contact numbering, symbol and full description.

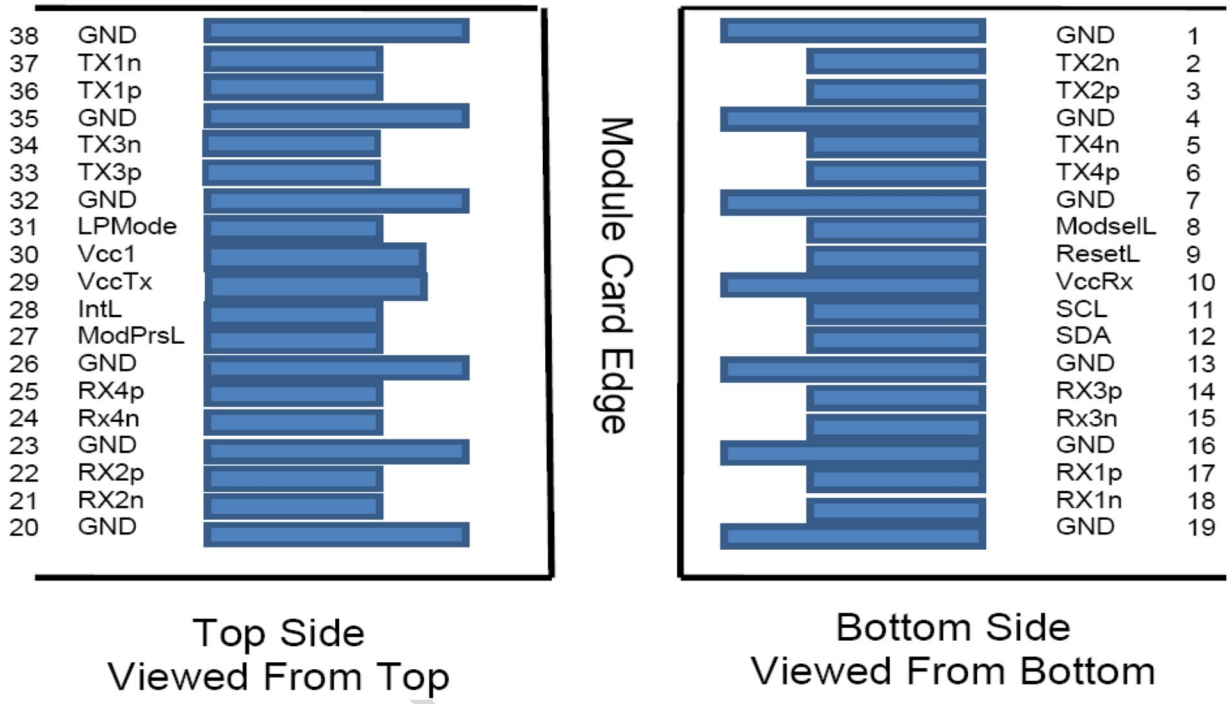


Figure 1. QSFP compliant 38-pin connector

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QSFP Transceiver Pinout

Pin No.	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1
2	CML-I	TX2n	Transmitted Inverted Data Input	3
3	CML-I	TX2p	Transmitted Non-Inverted Data Input	3
4		GND	Ground	1
5	CML-I	TX4n	Transmitted Inverted Data Input	3
6	CML-I	TX4p	Transmitted Non-Inverted Data Input	3
7		GND	Ground	1
8	LVTTL-I	ModSeil	Module Select	3
9	LVTTL-I	ResetL	Module Reset	3
10		Vcc Rx	+3.3 VDC Receiver Power Supply	2
11	LVCMOS-I/O	SCL	Serial Clock for I2C Interface	3
12	LVCMOS-I/O	SDA	Serial Data for I2C Interface	3
13		GND	Ground	1
14	CML-O	RX3p	Receiver Non-Inverted Data Output	3
15	CML-O	RX3n	Receiver Inverted Data Output	3
16		GND	Ground	1
17	CML-O	RX1p	Receiver Non-Inverted Data Output	3
18	CML-O	RX1n	Receiver Inverted Data Output	3
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	RX2n	Receiver Inverted Data Output	3
22	CML-O	RX2p	Receiver Non-Inverted Data Output	3
23		GND	Ground	1
24	CML-O	RX4n	Receiver Inverted Data Output	3
25	CML-O	RX4p	Receiver Non-Inverted Data Output	3
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	3
28	LVTTL-O	IntL	Interrupt	3
29		Vcc Tx	+3.3 VDC Transmitter Power Supply	2
30		Vcc1	+3.3 VDC Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	3
32		GND	Ground	1
33	CML-I	TX3p	Transmitted Non-Inverted Data Input	3
34	CML-I	TX3n	Transmitted Inverted Data Input	3
35		GND	Ground	1
36	CML-I	TX1p	Transmitted Non-Inverted Data Input	3
37	CML-I	TX1n	Transmitted Inverted Data Input	3
38		GND	Ground	1

Host Board Schematic

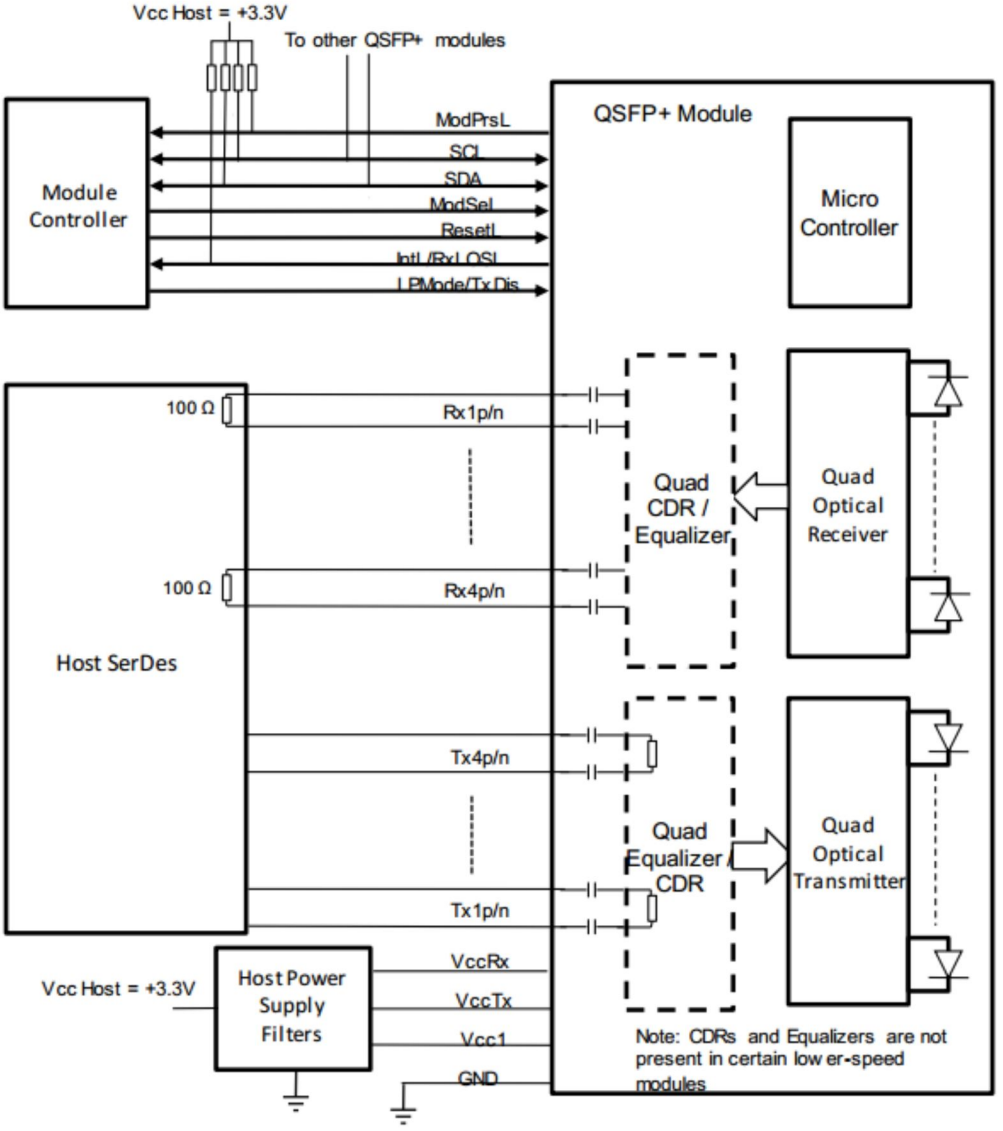


Figure 2. Host Board Schematic